



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/646,453

08/21/2003

John Thomas Welder

2705-0729

9544

73552

7590

06/08/2009

Stolowitz Ford Cowger LLP
621 SW Morrison St
Suite 600
Portland, OR 97205

EXAMINER

RUTTEN, JAMES D

ART UNIT

PAPER NUMBER

2192

MAIL DATE

DELIVERY MODE

06/08/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/646,453	Applicant(s) WELDER ET AL.	
	Examiner JAMES RUTTEN	Art Unit 2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-44 have been examined.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 6, 8-10, 15-20, 23, 25-29, 32, 34-38, 41, and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,639,910 to Provencher et al. ("Provencher") in view of "Networking Explained, Second Edition" by Gallo et al. ("Gallo").

In regard to claim 1, Provenchar discloses:

A method of resetting an electronic device (see column 9 lines 30-32, i.e. "reset") comprising:

a) separating software operations associated with layer two of an International Standardization Organization Open Systems Interconnect (ISO/OSI) reference model from other layers in said ISO/OSI reference model, said electronic device implementing said software operations; See column 3 line 66 through line 8, e.g. "That is, the control plane and the data plane have separate processor subsystems that do not share processing cycles. Such a device architecture can be implemented by employing either monolithic or modular software architecture." Provenchar does not expressly disclose the ISO/OSI

Art Unit: 2192

reference model. However, Gallo teaches that an OSI reference layer 2 relates to data link. See page 44, Figure 2.10, e.g. "Data Link (2)." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Provenchar's data plane with Gallo's OSI model in order to utilize a standard architecture as suggested by Gallo (see page 42, Question 34.).

b) resetting said software operations in said layer two of said electronic device;

See column 9 lines 30-32, e.g. "reset the subsystems in the data plane."

c) maintaining continuity for a communication session between said electronic

device and other electronic devices coupled together through a network; and See

column 6 lines 13-18, e.g. "Hence, a malfunction of one or more of the forwarding subsystems does not affect the proper functioning of the physical connection subsystems. Similarly, a malfunction of one or more of the physical connection systems does not affect the proper functioning of the forwarding subsystems." For the same reasons in the cited text, a reset of the data plane would also maintain continuity.

d) recovering execution of said software operations at said layer two before said

continuity of said communication session is terminated. See column 3 lines 46-50,

column 9 lines 24-32 and column 10 lines 64-67. These passages provide implicit disclosure of the claim limitation as it describes continuity of system operation while the software is reset. That is, the communication sessions are not terminated.

In regard to claim 2, the above rejection of claim 1 is incorporated. Provenchar further discloses: *wherein a) further comprises: a1) separating a data plane and a*

Art Unit: 2192

control plane in said electronic device, See column 3 line 66 through line 8, e.g. "That is, the control plane and the data plane have separate processor subsystems that do not share processing cycles. Such a device architecture can be implemented by employing either monolithic or modular software architecture. Provenchar does not expressly disclose: *said data plane being associated with said layer two, and said control plane being associated with layers above said layer two of said ISO/OSI reference model*. However, Gallo teaches that layer two of the OSI model relates to the link layer and data transfer, while layer 3 relates to networking and routing of data. It would have been obvious to one of ordinary skill in the art at the time the invention was made to associate Provenchar's data and control planes with Gallo's OSI layers 2 and above in order to simplify design as suggested by Gallo (see page 43, question 36).

In regard to claim 3, the above rejection of claim 1 is incorporated. Provenchar further discloses: *wherein c) further comprises: c1) maintaining continuity at layer one of said ISO/OSI reference model; and c2) maintaining continuity at layers above said second layer of said ISO/OSI reference model*. See column 6 lines 13-18, e.g. "Hence, a malfunction of one or more of the forwarding subsystems does not affect the proper functioning of the physical connection subsystems. Similarly, a malfunction of one or more of the physical connection systems does not affect the proper functioning of the forwarding subsystems." For the same reasons in the cited text, continuity is maintained among the layers. As noted above, Provenchar does not expressly disclose details regarding the OSI reference model. However, these are made obvious by Gallo.

In regard to claim 6, the above rejection of claim 1 is incorporated. Provenchar further discloses: *wherein b) further comprises: b1) performing a minimal reset of hardware components associated with said layer two such that interruptions to an operating system of said electronic device are minimized.* See column 9 line 31, e.g. "reset the subsystems." Note that only the subsystems are reset, thereby minimizing interruption.

In regard to claim 8, the above rejection of claim 1 is incorporated. Provenchar does not expressly disclose: *wherein said network comprises the Internet.* However, Provenchar discloses use of the Internet Protocol ("IP"). See column 2 lines 45-46. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Provenchar's use of IP with the Internet in order to utilize a well-known network which is built upon the use of IP.

In regard to claim 9, the above rejection of claim 1 is incorporated. Provenchar further discloses: *wherein said electronic device comprises a network device.* See column 1 line 33, e.g. "network device."

In regard to claim 10, Provenchar discloses a method of resetting an electronic device (see at least column 9 lines 30-32, i.e. "reset"). All further limitations have been addressed in the above rejections of claims 1-3, respectively.

In regard to claim 15, the above rejection of claim 10 is incorporated. All further limitations have been addressed in the above rejection of claim 6.

In regard to claim 16, the above rejection of claim 15 is incorporated. Provenchar further discloses: *wherein d) further comprises: resuming operations of said hardware components.* See at least column 9 lines 30-32, i.e. "reset."

In regard to claim 17, the above rejection of claim 10 is incorporated. All further limitations have been addressed in the above rejection of claim 9.

In regard to claim 18, Provenchar disclose:

A computer system comprising: a processor; and a computer readable memory coupled to said processor and containing program instructions. See at least Fig. 1 and column 8 lines 63-65, e.g. "processors and memory." All further limitations have been addressed in the above rejection of claim 1.

In regard to claims 19-20, 23 and 25-26, the above rejection of claim 18 is incorporated. All further limitations have been addressed in the above rejections of claims 2-3, 6, and 8-9, respectively.

Art Unit: 2192

In regard to claim 27, Provenchar discloses: *a system for resetting an electronic device*. See Fig. 1. All further limitations have been addressed in the above rejection of claim 1.

In regard to claims 28-29, 32, and 34-35, the above rejection of claim 27 is incorporated. All further limitations have been addressed in the above rejections of claims 2-3, 6, and 8-9, respectively.

In regard to claim 36, Provenchar discloses: *A computer-readable medium comprising computer-executable instructions*. See at least column 8 lines 63-65, e.g. processors and memory. All further limitations have been addressed in the above rejection of claim 1.

In regard to claims 37-38, 41 and 43-44, the above rejection of claim 36 is incorporated. All further limitations have been addressed in the above rejections of claims 2-3, 6, and 8-9, respectively.

4. Claims 4, 11, 13-14, 21, 30, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Provenchar and Gallo and further in view of U.S. Patent Application Publication No. US 2003/0084440 by Lownes ("Lownes").

In regard to claim 4, the above rejection of claim 1 is incorporated. Provenchar further discloses: *wherein b) further comprises: b1) ...new software implementing said software operations to a first memory location of said electronic device;* See column 9 line 27, i.e. "upgrade." Povenchar and Gallo do not expressly disclose: *...pre-loading ... and b2) loading a bootstrap code to a second memory location of said electronic device, said bootstrap code for loading said new software to a predetermined location, said predetermined location storing existing software implementing said software operations.* However, Lownes teaches pre-loading updates and using bootstrap code for loading new software. See paragraph [0043]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Provenchar's update with Lownes' pre-loading in order to utilize a checksum verification as suggested by Lownes.

In regard to claim 11, the above rejection of claim 10 is incorporated. All further limitations have been addressed in the above rejection of claim 4.

In regard to claim 13, the above rejection of claim 11 is incorporated. Provenchar further discloses: *wherein b1) further comprises: upgrading said software operations that are implemented within said new software.* See column 1 lines 33-37.

In regard to claim 14, the above rejection of claim 11 is incorporated. Provenchar further discloses: *wherein b1) further comprises: reloading said software operations that are implemented within said new software.* See column 2 lines 16-24.

In regard to claim 21, the above rejection of claim 18 is incorporated. All further limitations have been addressed in the above rejection of claim 4.

In regard to claim 30, the above rejection of claim 27 is incorporated. All further limitations have been addressed in the above rejection of claim 4.

In regard to claim 39, the above rejection of claim 36 is incorporated. All further limitations have been addressed in the above rejection of claim 4.

5. Claims 5, 12, 22, 31, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Provenchar, Gallo, and Lownes, and further in view of U.S. 5,263,168 to Toms et al. ("Toms").

In regard to claim 5, the above rejection of claim 4 is incorporated. Provenchar does not expressly disclose: *wherein d) further comprises: d1) executing said bootstrap code by moving a program counter of said electronic device to a first beginning instruction of said bootstrap code to overwrite said existing software at said predetermined location with said new software; and d2) executing said new software by moving said program counter to a second beginning instruction of said new software to initialize said new software.* Lownes discloses *overwrite said existing software at said predetermined location with said new software;* See paragraph [0043]. Provenchar,

Art Unit: 2192

Gallo, and Lownes do not expressly disclose features related to a program counter.

However, Toms teaches the well known use of a program counter to execute code. See column 1 lines 21-24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Provenchar's update and Lownes' bootstrap with Toms' teaching of a program counter in order to indicate a starting address of a software program as suggested by Toms.

In regard to claim 12, the above rejection of claim 11 is incorporated. All further limitations have been addressed in the above rejection of claim 5.

In regard to claim 22, the above rejection of claim 21 is incorporated. All further limitations have been addressed in the above rejection of claim 5.

In regard to claim 31, the above rejection of claim 30 is incorporated. All further limitations have been addressed in the above rejection of claim 5.

In regard to claim 40, the above rejection of claim 39 is incorporated. All further limitations have been addressed in the above rejection of claim 5.

6. Claims 7, 24, 33, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Provenchar, and Gallo, and further in view of U.S. 6,658,659 to Hiller et al. ("Hiller").

Art Unit: 2192

In regard to claim 7, the above rejection of claim 6 is incorporated. Provenchar does not expressly disclose: *wherein at least one of said hardware components comprises a line card*. However, Hiller teaches that line cards are used as interfaces. See column 14 lines 10-11, e.g. "line cards." It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Provenchar's hardware components with Hiller's line cards in order to utilize a device for sending and receiving of data packets as suggested by Hiller (see column 14 lines 11-14).

In regard to claim 24, the above rejection of claim 23 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

In regard to claim 33, the above rejection of claim 32 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

In regard to claim 42, the above rejection of claim 41 is incorporated. All further limitations have been addressed in the above rejection of claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES RUTTEN whose telephone number is (571)272-3703. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. Derek Rutten/
Examiner, Art Unit 2192